Amendments to the Specification:

Please replace the paragraph starting at page 1, line 7 and ending at line 11 with the following amended paragraph:

The invention relates to an apparatus for generating pseudo-noise codes, and in particular to an apparatus for generating pseudo-noise codes adapted for advancing or retarding 1 pseudo-noise chip generated therefrom within one clock cycle in a radio communication network based on ~~the~~ code division multiple access(CDMA), and a method for generating pseudo-noise codes by using the pseudo-noise code generating apparatus.

Please replace the paragraph starting at page 1, line 20 and ending at page 2, line 3 with the following amended paragraph:

In IS-95 as the international standard of the CDMA communication system, ~~an~~ a Long PN code generator for $(2^{42}-1)$ beat length and a short PN code generator for 2^{15} are currently recommended. Herein, the short PN code generator generates short PN code lines of 2^{15} beat length in respect to each of an in-phase (hereinafter will referred to I) channel and a quadrature-phase (hereinafter will be referred to Q) channel.

Please replace the paragraph starting at page 2, line 8 and ending at line 15 with the following amended paragraph:

The PIN codes generated from these pseudo noise code generators are generated by ~~an~~ a Linear sequence shift register (hereinafter will be referred to LSSR) composed of n number of flip-flops of shift registers. In particular, the pseudo noise code generators are applied so that a searcher of a base station receiver or terminal receiver can rapidly acquire pilot signals included in the received signals and a finger of the receiver can track the PN codes included in the received signals. Here, the PN codes are generated by the pseudo noise

code generator to find PN codes included in the received signals in the receiver of the base station or terminal, and offsets of the PN codes are intentionally retarded or advanced to perform operations for acquiring pilot signals or finding the PN codes.

Please replace the paragraph starting at page 8, line 1 and ending at line 3 with the following amended paragraph:

First, an input value is obtained as a result of OR operating the output signal of the (i-1)th shift register and a resultant value of an AND operation of an output signal of the nth shift register and the (i-1)th value of the generation polynomial given to the PN code generator.

Please replace the equation at page 8, line 9 with the following amended equation:

$$r_{i,m+2} = \begin{cases} r_{i-2,m} \oplus (r_{n,m} g_{i-2}) \oplus \left[\{r_{n-1,m} \oplus (r_{n,m} g_{n-1})\} g_{i-1}\right], & 0 < i \le n, \text{wherein } i \text{ is an integer} \\ r_{n-1,m} \oplus (r_{n,m} g_{n-1}) & , i = 1 \\ 0 & , i = 0 \end{cases}$$

$$r_{i,m+2} = \begin{cases} r_{i-2,m} \oplus (r_{n,m} g_{i-2}) \oplus \left[\{r_{n-1,m} \oplus (r_{n,m} g_{n-1})\} g_{i-1}\right], & 1 < i \le n, \text{wherein } i \text{ is an integer} \\ r_{n-1,m} \oplus (r_{n,m} g_{n-1}) & , i = 1 \\ 0 & , i = 0 \end{cases}$$

Please replace the paragraph starting at page 9, line 3 and ending at line 9 with the following amended paragraph:

Also, a resultant value is input to the input end of the random ith shift register of shift registers from 2 to n, which is obtained through an OR operation of a first value which is obtained by an AND operation of the (i-1)th value of the generation polynomial and a value from an OR operation of an output signal of the (n-1)th shift register and a value from an AND operation of an output signal of the nth shift register and the (n-1)th value of the generation polynomial; a second value which is obtained through an AND operation of an output signal of the nth shift register with the (i-2)th value of the generation polynomial; and a third value as an output signal of the (i-2)th shift register.

Please replace the paragraphs starting at page 11, line 7 and ending at page 11, line 13 with the following amended paragraphs:

FIG. 5 is a block diagram for showing the configuration of the PN code generator according to the first embodiment of the invention.

In FIG 5, the block diagram of the PIN code generator is given with generation polynomial $g(X) = X^4 + X^3 + 1$, and has a combined configuration of FIG. 2 and FIG. 3.

In other words, a combination is provided by ~~means of~~ a circuit for obtaining the next state of the LSSR in the normal state and another circuit for obtaining the next state of the LSSR to perform one PN chip advance.

Please replace the paragraphs starting at page 11, line 20 and ending at page 12, line 14 with the following amended paragraphs:

Herein, "0" which is one input of the MUX 21 connected to the input end of the first LSSR of the 4 LSSRs is defined as an output value of the forth LSSR14, and "1" [[or]] of the

other input of the MUX 21 is defined as a value obtained by OR operating an output signal of the fourth LSSR 14 and an output signal of the third LSSR 13 by an adder 15.

Also, "0" is one input of the MUX 23 connected to the input end of the random ith (herein i is an integer between 2 to n) LSSR, for example, the third LSSR 13 in which i=3, except the first LSSR 11 of 4 LSSRs 11 to 14, and is defined as a value obtained from an OR operation of an output value of the second((i-1)th) shift register 12 with an AND operated value of an output value of the fourth shift register 14 with an output value of the second shift register 12. "1" is another input of the MUX 23 connected to the input end of the third shift register 13 and is defined as a resultant value obtained from an OR operation of first, second and third values~~, in which the~~. The first value is obtained from an AND operation of ~~a~~ an (i-1)th value ~~of AND operation of second value of~~ of the generation polynomial (i.e., the second value of the generation polynomial) and a value from an OR operation of an output signal of the (n-1)th shift register (i.e., the third shift register 13) and a value from an AND operation of output signal of the nth shift register (i.e., the fourth shift register 14) and the (n-1)th (i.e., the third value) of the generation polynomial, the second value is obtained from ~~OR~~ an AND operation of an output signal of the nth shift register (i.e., the fourth shift register 14) and the (i-2)th value of the generation polynomial (i.e., the first value of generation polynomial), and the third value is an output value of the (i-2)th shift register (i.e., the first shift register). See also equation 7 for mathematical expressions of the first, second and third values.

Please replace the paragraph starting at page 13, line 3 and ending at line 5 with the following amended paragraph:

FIG. 6 is a block diagram for showing the configuration of a PN code generator according to the second embodiment of the invention.

Please replace the paragraphs starting at page 13, line 7 and ending at page 15, line 1 with the following amended paragraphs:

In other words, in FIG. 6, a first circuit for obtaining the next state of the LSSR in the normal state, a second circuit for obtaining the next state of the LSSR to perform one PN chip advance, and a third circuit for obtaining the next state of the LSSR to perform one PN chip retard are combined. The PN code generator according to the second embodiment of the invention is provided with [[an]] a Load enable signal, and is comprised of 4 shift registers 11 to 14 serially connected with each other; 4 MUXs 21 to 24 for outputting one input signal out of multiple input signals according to each control signal, each of the MUXs 21 to 24 being connected to the input end of each of the shift registers 11 to 14; and an encoder 31 for generating a control signal to set the state of the PN code generator to 4 MUXs 21 to 24.

Herein, "0" is one input of the MUX 21 connected to the input end of the first shift register 11 of the shift registers and is defined as an output value of the ~~forth~~ fourth LSSR 14. "1" is another input of the MUX 21 and is defined as a value of an OR operation of an output value of the fourth shift register 14 and an output value of the third shift register 13 by an ~~AN~~ adder 15. "2" is ~~further~~ another input of the MUX 21 and is defined as an output signal of the shift register 11.

Also, "0" is one input of the MUX 23 connected to the input end of the random ith (herein i is an integer between 2 to n) LSSR, for example, the third LSSR 13 in which i=3, except the first LSSR 11 of 4 LSSRs 11 to 14, and is defined as a value obtained from an OR operation of an output value of the second((i-1)th) shift register 12 with an AND operated value of an output value of the fourth shift register 14 with an output value of the second shift register 12. "1" is another input of the MUX 23 connected to the input end of the third shift register 13 and is defined as a resultant value obtained from an OR operation of first,

second and third values~~, in which the~~. The first value is obtained from an AND operation of ~~a~~ an (i-1)th value ~~of AND operation of second value of~~ of the generation polynomial (i.e., the second value of the generation polynomial) and a value from an OR operation of an output signal of the (n-1)th shift register (i.e., the third shift register 13) and a value from an AND operation of output signal of the nth shift register (i.e., the fourth shift register 14) and the (n-1)th (i.e., the third value) of the generation polynomial, the second value is obtained from ~~OR~~ an AND operation of an output signal of the nth shift register (i.e., the fourth shift register 14) and the (i-2)th value of the generation polynomial (i.e., the first value of generation polynomial), and the third value is an output value of the (i-2)th shift register (i.e., the first shift register). "2" is ~~further~~ another input of the MUX 23 connected to the input end of third shift register 13 and is defined as an output signal of third shift register 13.

In FIG. 6, it can be seen that output sequences from FIG. 2 to FIG. 4 can be collected to each of the MUXs 21 to 24 and a control signal (MUX_SEL) applied from an encoder can be used to control an output of each of the MUXs 21 to 24.

Therefore, the receiving end of the transmitter can treat a desired one selected from ~~group including~~ an operation in the normal state of the PN code generator, one PN chip advance operation [[and]] or one PN chip retard operation within one clock.

FIG. 7 is a block diagram for showing the configuration of an LSSR of a PN code generator according to the third embodiment of the invention, and FIG. 8 illustrates an operation of generating PN codes of the PN code generator shown in FIG. 7.

Please replace the paragraph starting at page 15, line 17 and ending at page 16, line 1 with the following amended paragraph:

FIG. 9 shows the configuration of comparators for comparing the present load state

and the next load state of the LSSR for generating the PN codes of the invention shown in FIG. 7, FIG. 10 shows the configuration of the MUX and a flip-flop for outputting load commands from each output of the comparators shown in FIG. 9 and index shown in table 1, FIG. 11 shows a decoder for controlling the MUX shown in FIG. 7, and FIG. 12 shows the overall configuration of the PN code generator according to the third embodiment of the invention shown in FIG. 7 to FIG. 11.

Please replace the paragraph starting at page 20, line 11 and ending at line 17 with the following amended paragraphs:

Accordingly, the MUXs 10 to 13 are controlled from one PN chip advanced or one PN chip retarded input as in FIG. 7 and FIG. 8 of the invention so that one PN chip advance and retard including a normal operation of PN code generation can be treated within one clock cycle.

In other words, the present PN state is the LSB in the left side and the MSB in the right side of the LSSR output. Here, when '10' (0010 the next state of 0100) is first output, the MUX control input (MC) signal is 0, so it is a retard state of repeating the present state once more, and when '10' is second output, the MUX control input (MC) signal is 1 to pass to the next state output.